Amendments to the Specification

Please amend the specification as follows.

Please amend the paragraph of the clean copy of the substitute specification filed on June 28, 2006 starting at page 17, line 25 as follows:

Figure 1 is a block diagram illustrating the construction of a clock conversion apparatus according to the first embodiment. In Figure 1, reference numeral 101 denotes a write address counter for controlling write addresses. The write address counter 101 starts up-counting of a first clock (clock for writing) S109 by a horizontal sync pulse signal (writing start reference signal) S101, and outputs write addresses S102 of a memory 107 as count values. The write address counter 101 is once reset by the next horizontal sync pulse signal S101, and starts the next up-counting. Reference numeral 102 denotes a write maximum value limiter (maximum value limiter circuit) for write addresses. The write maximum value limiter 102 resets the write address counter 101 by a write address reset signal S103 when the write address S102 becomes equal to a value that is set by a maximum value control signal S112. Reference numeral 10 denotes a first counter circuit comprising the write address counter 101 and the write maximum value limiter 102. The first counter circuit 10 counts the first clock S109, and creates write addresses S102 of the memory 107 so that data corresponding to one horizontal period (predetermined period), i.e., one horizontal sync line of data, can be written in the memory 107 over plural times ~~(i.e., using at least a portion of the addresses of the memory 107 a plurality of times)~~. The first counter circuit 10 creates the write addresses S102 so that up-counting is repeated within a predetermined range of addresses of the memory 107 as shown in Figure 7, or the last up-counting in one horizontal period is carried out within a range narrower than the predetermined range of addresses as shown in Figures 4～6 and 8.